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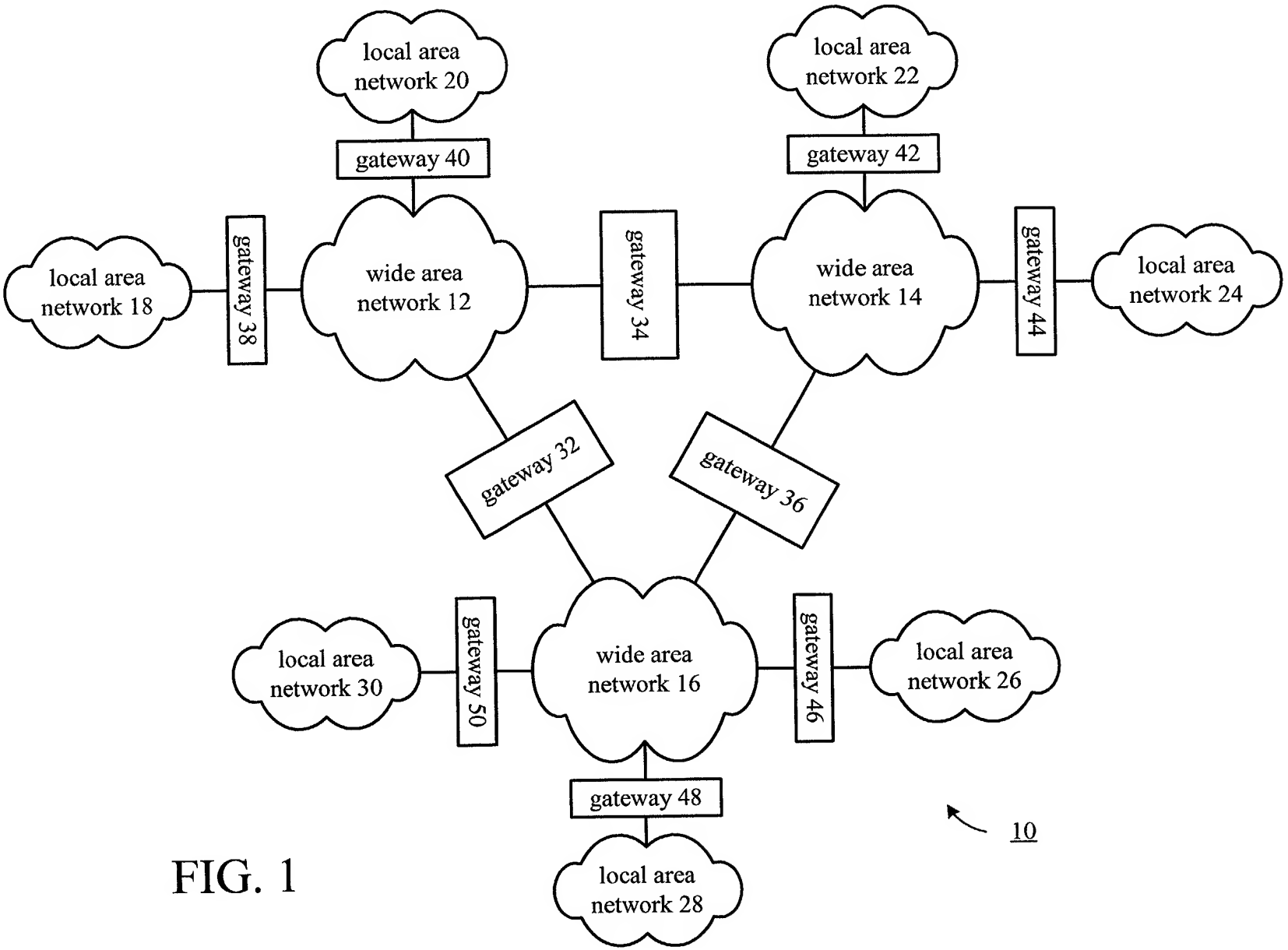

FIG. 1

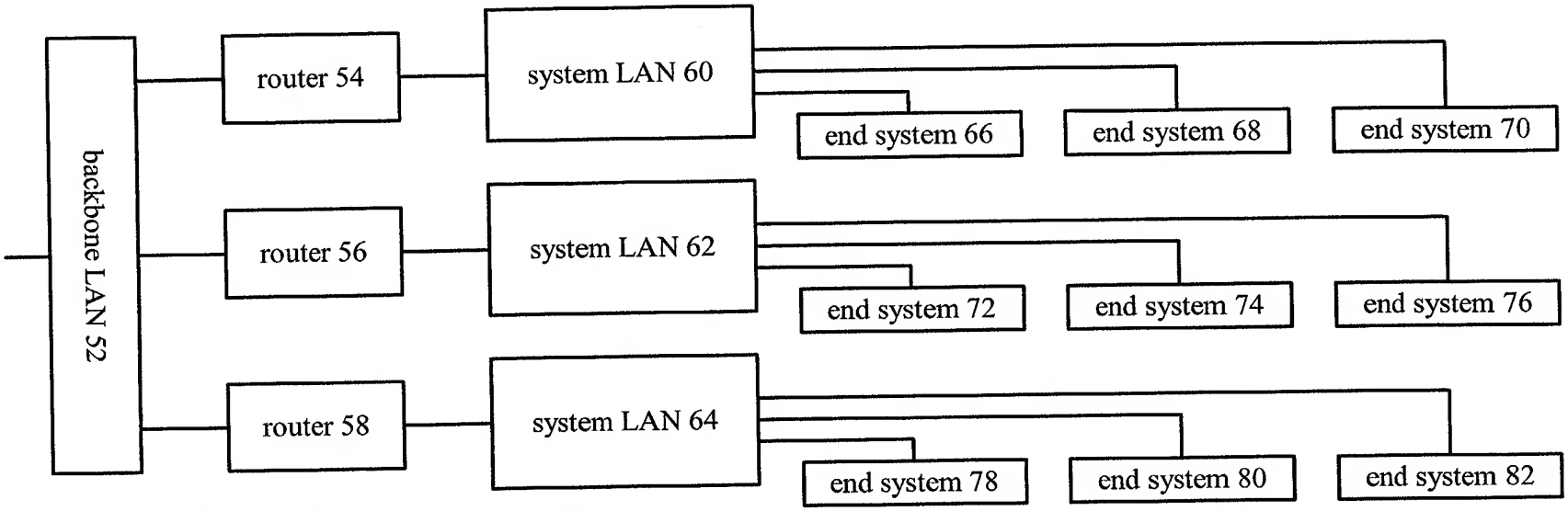

FIG. 2

LAN 18 - 30

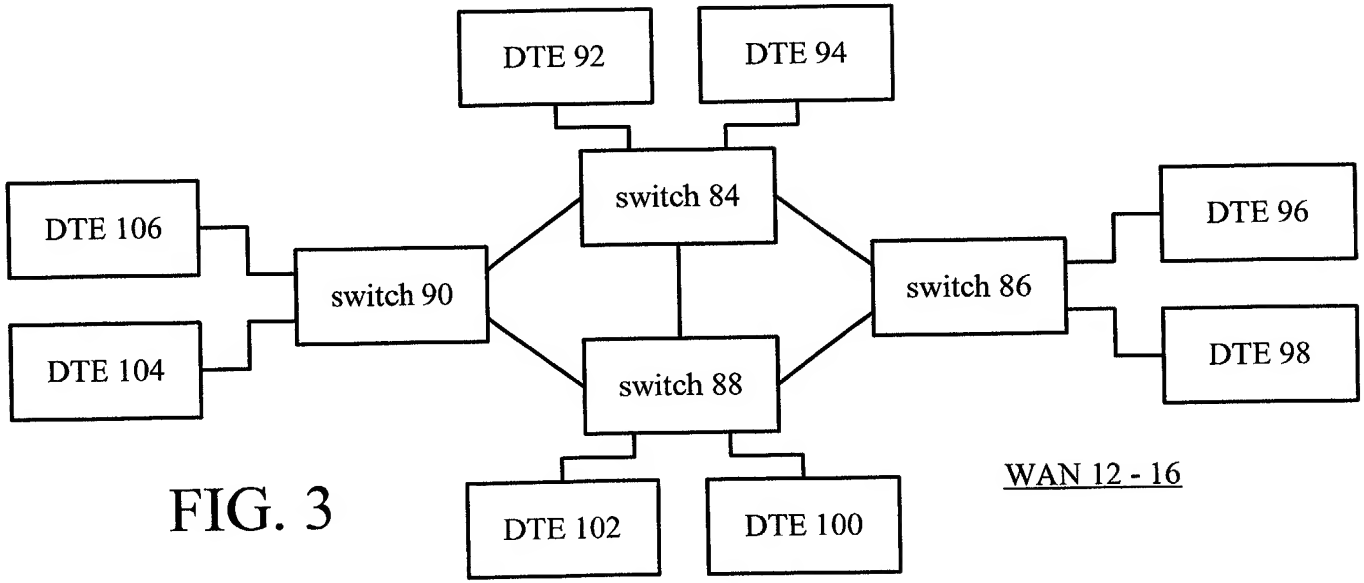

FIG. 3

WAN 12 - 16

20060726.0007

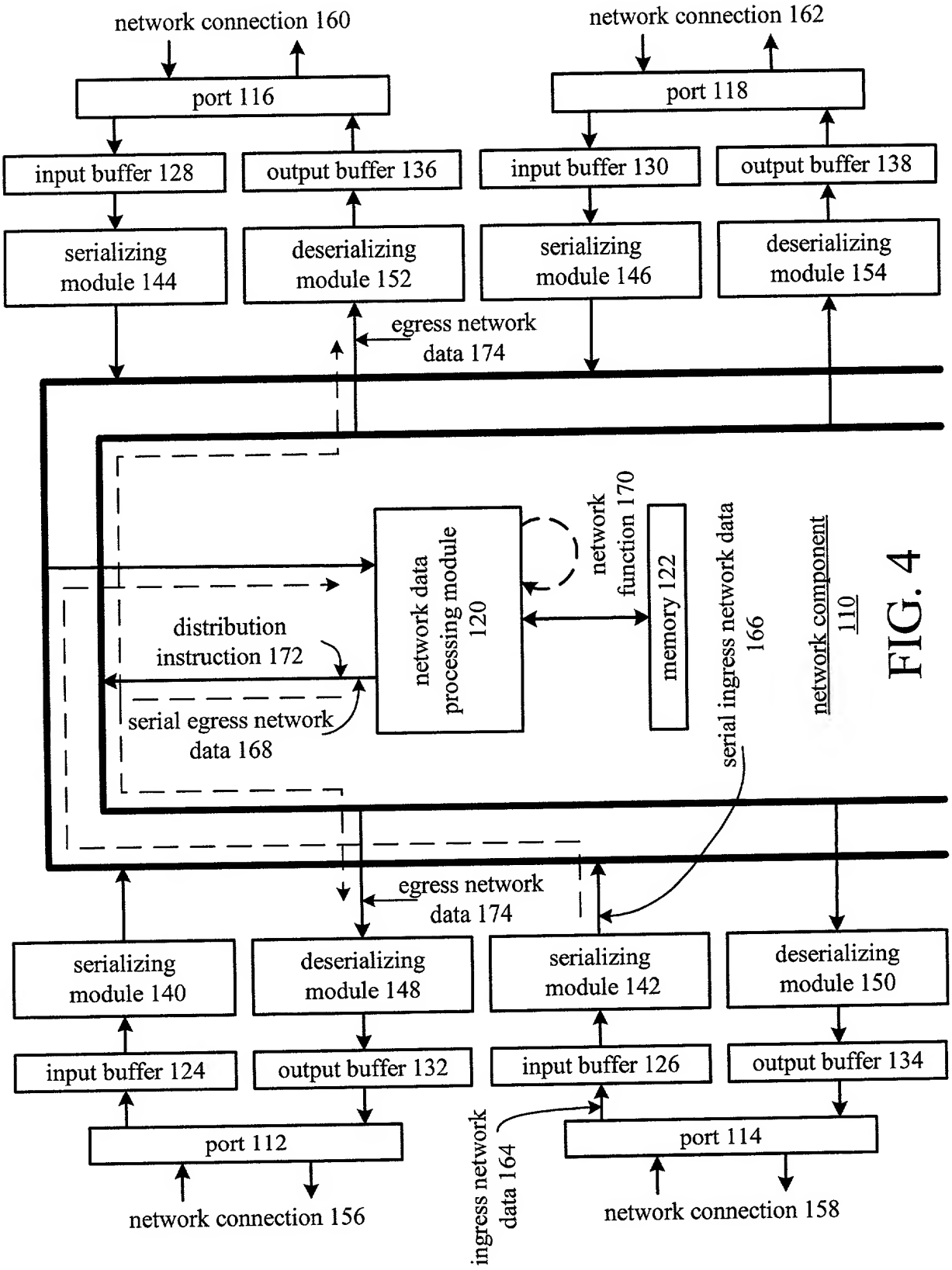

FIG. 4

PHOTO "H026001"

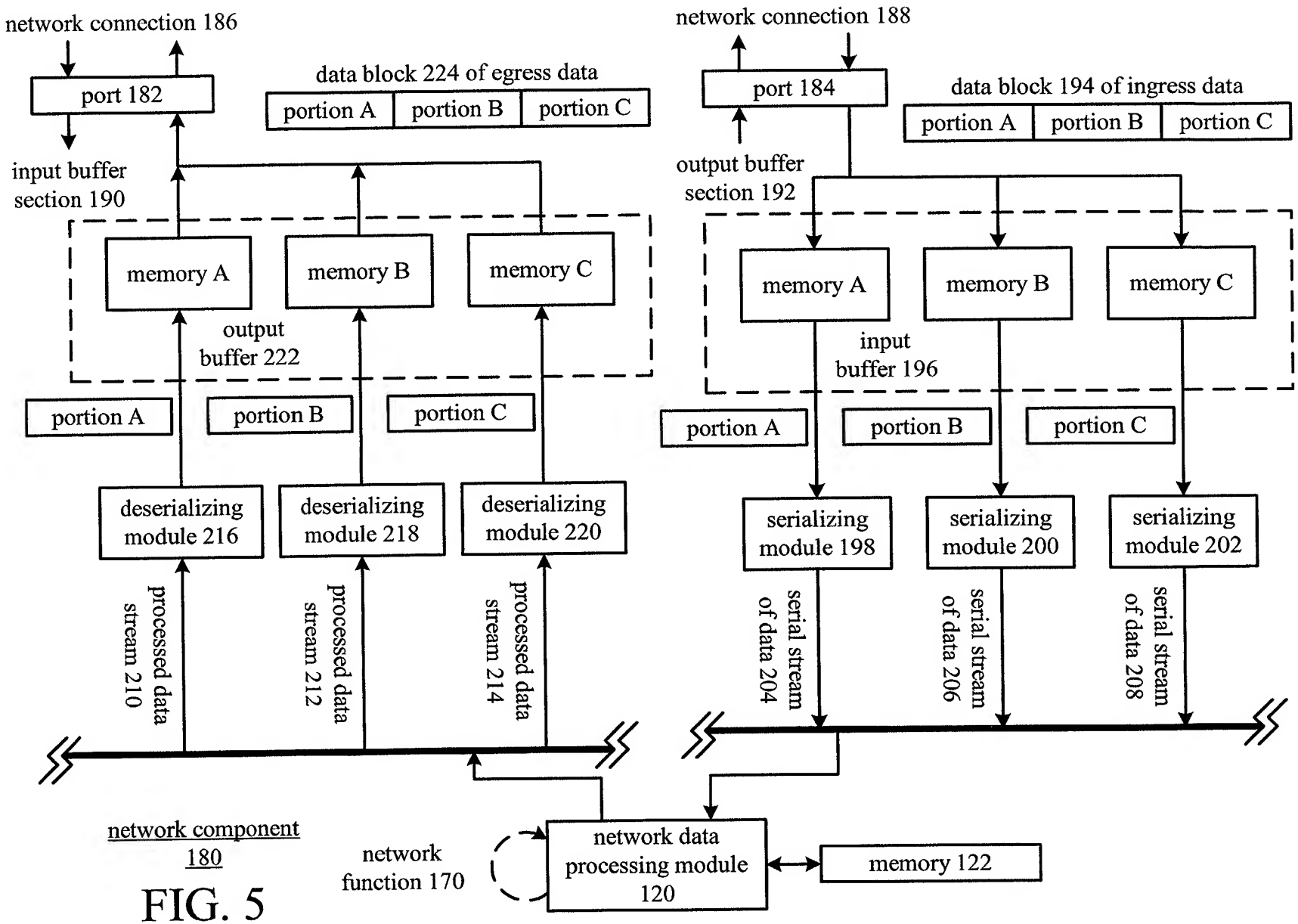

FIG. 5

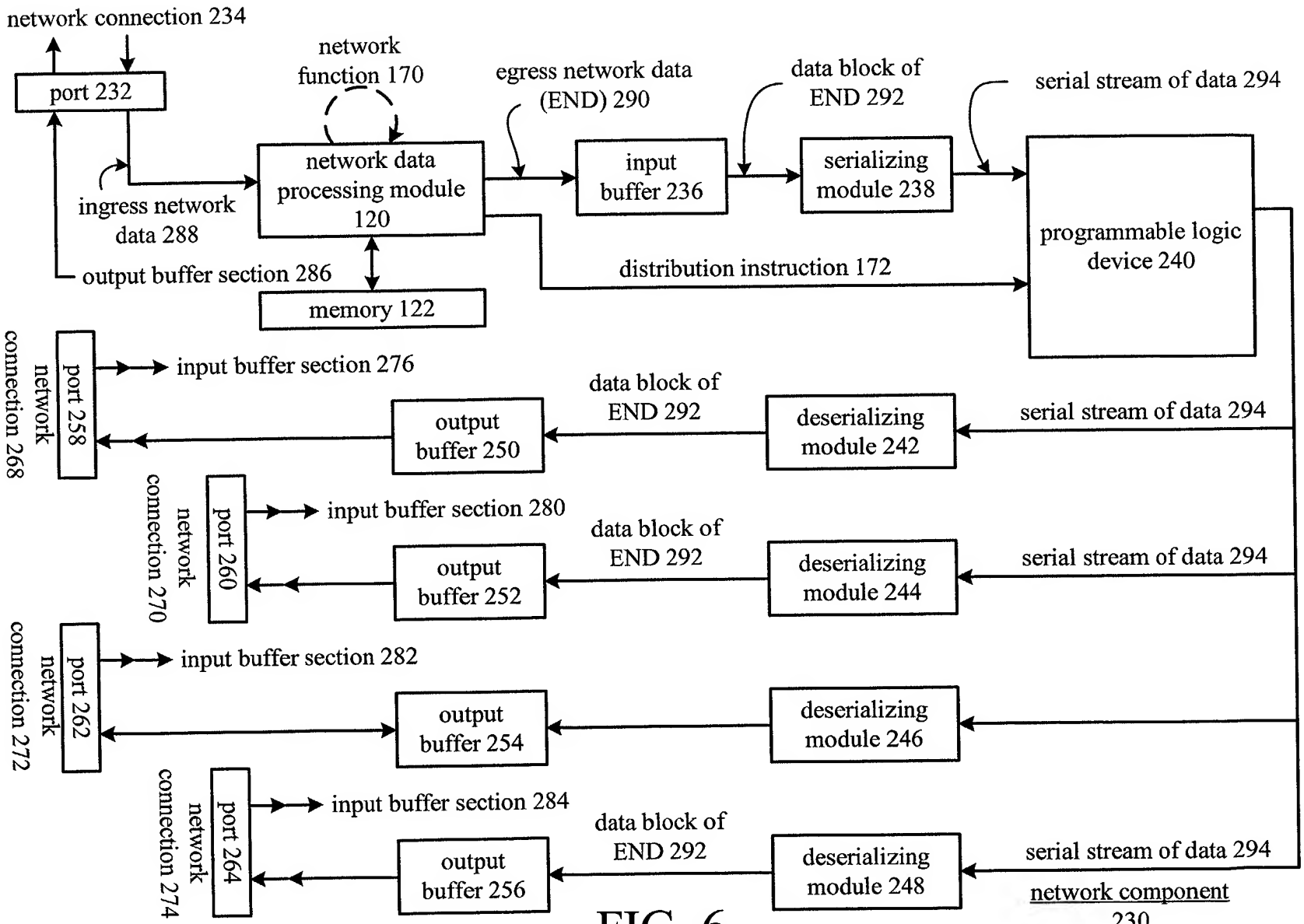
network connection 234
port 232
network function 170
egress network data (END) 290
data block of END 292
serial stream of data 294
network data processing module 120
input buffer 236
serializing module 238
programmable logic device 240
ingress network data 288
output buffer section 286
memory 122
distribution instruction 172
network connection 268
port 258
input buffer section 276
output buffer 250
data block of END 292
deserializing module 242
serial stream of data 294
network connection 270
port 260
input buffer section 280
output buffer 252
data block of END 292
deserializing module 244
serial stream of data 294
network connection 272
port 262
input buffer section 282
output buffer 254
deserializing module 246
network connection 274
port 264
input buffer section 284
output buffer 256
data block of END 292
deserializing module 248
serial stream of data 294
network component 230

FIG. 6

20070726007

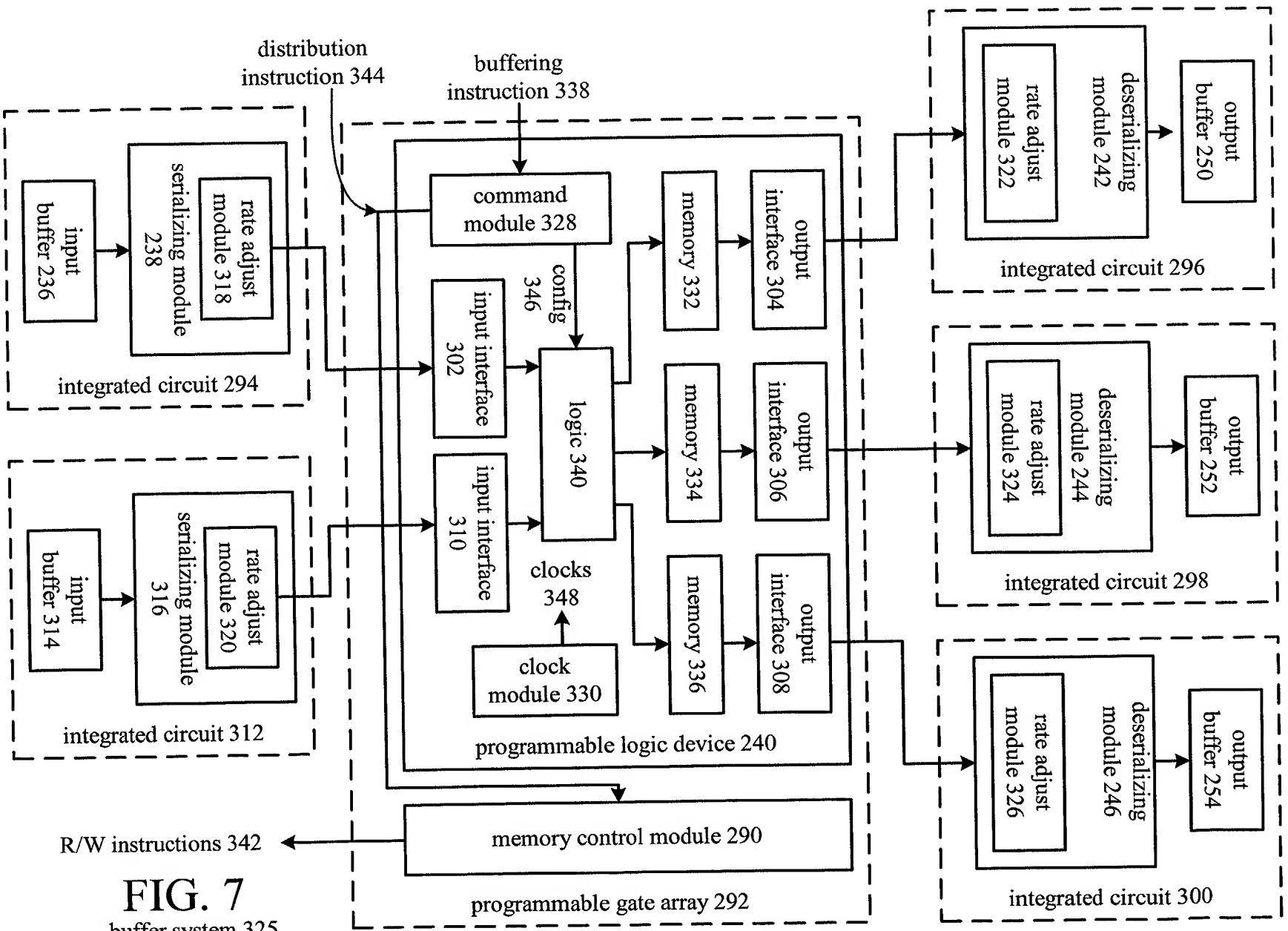

FIG. 7

buffer system 325

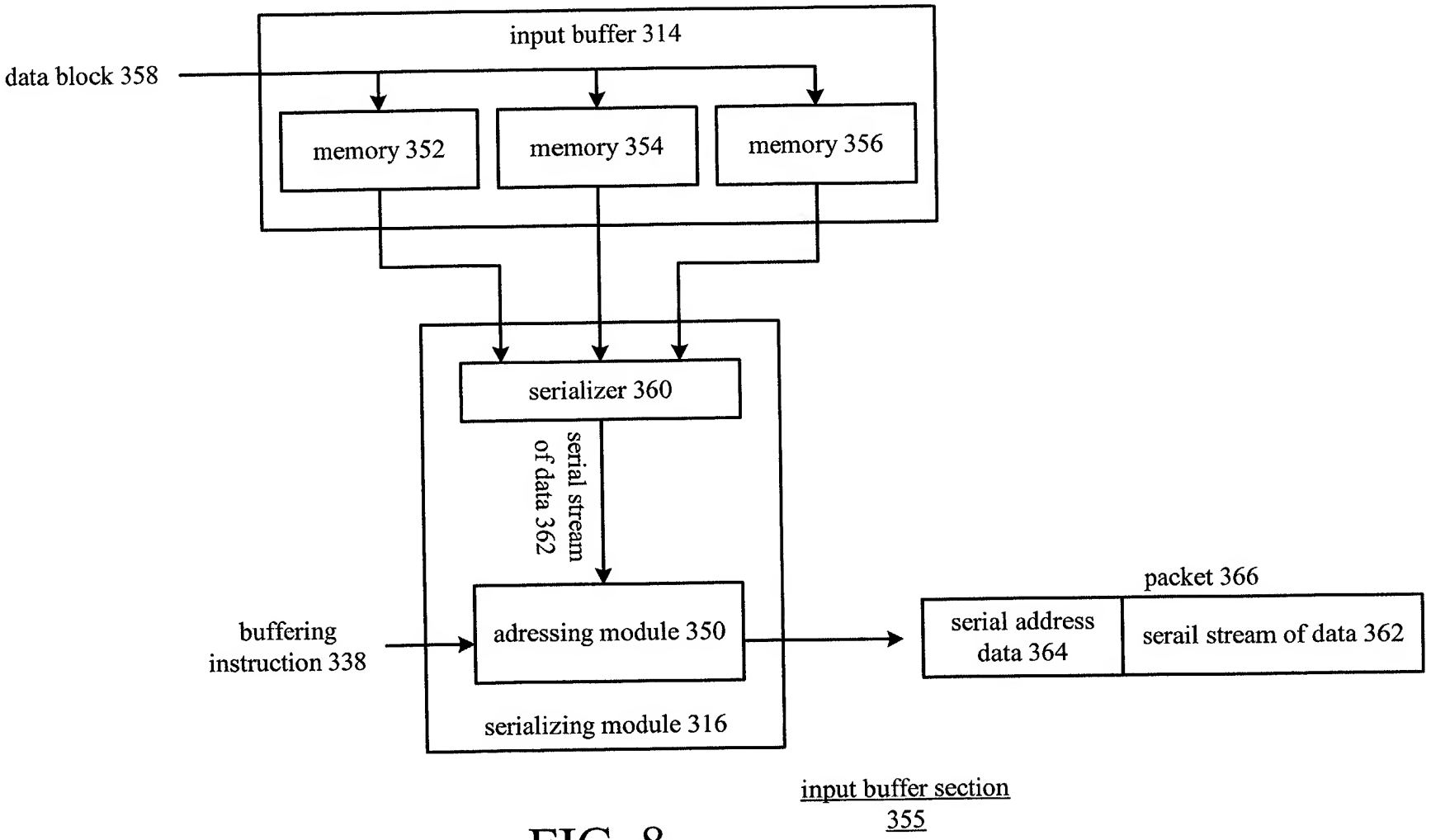
input buffer 314
data block 358
memory 352
memory 354
memory 356
serializer 360
serial stream of data 362
packet 366
buffering instruction 338
adressing module 350
serial address data 364
serail stream of data 362
serializing module 316
input buffer section 355

FIG. 8

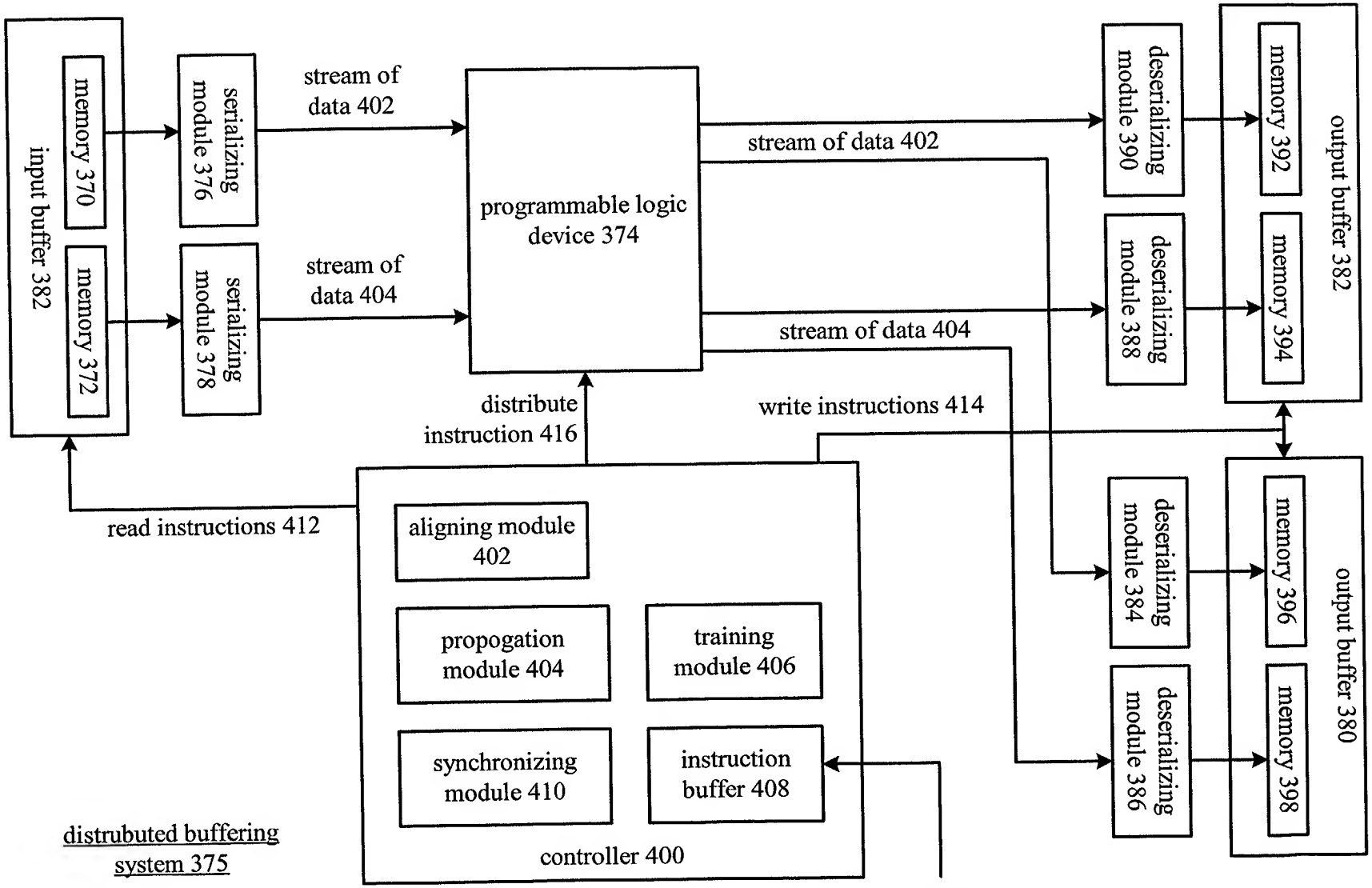
input buffer 382
memory 370
memory 372
serializing module 376
serializing module 378
stream of data 402
stream of data 404
programmable logic device 374
stream of data 402
stream of data 404
deserializing module 390
deserializing module 388
deserializing module 384
deserializing module 386
output buffer 382
memory 392
memory 394
output buffer 380
memory 396
memory 398
distribute instruction 416
write instructions 414
read instructions 412
aligning module 402
propogation module 404
training module 406
synchronizing module 410
instruction buffer 408
controller 400
distrubuted buffering system 375
buffering instruction 418

FIG. 9

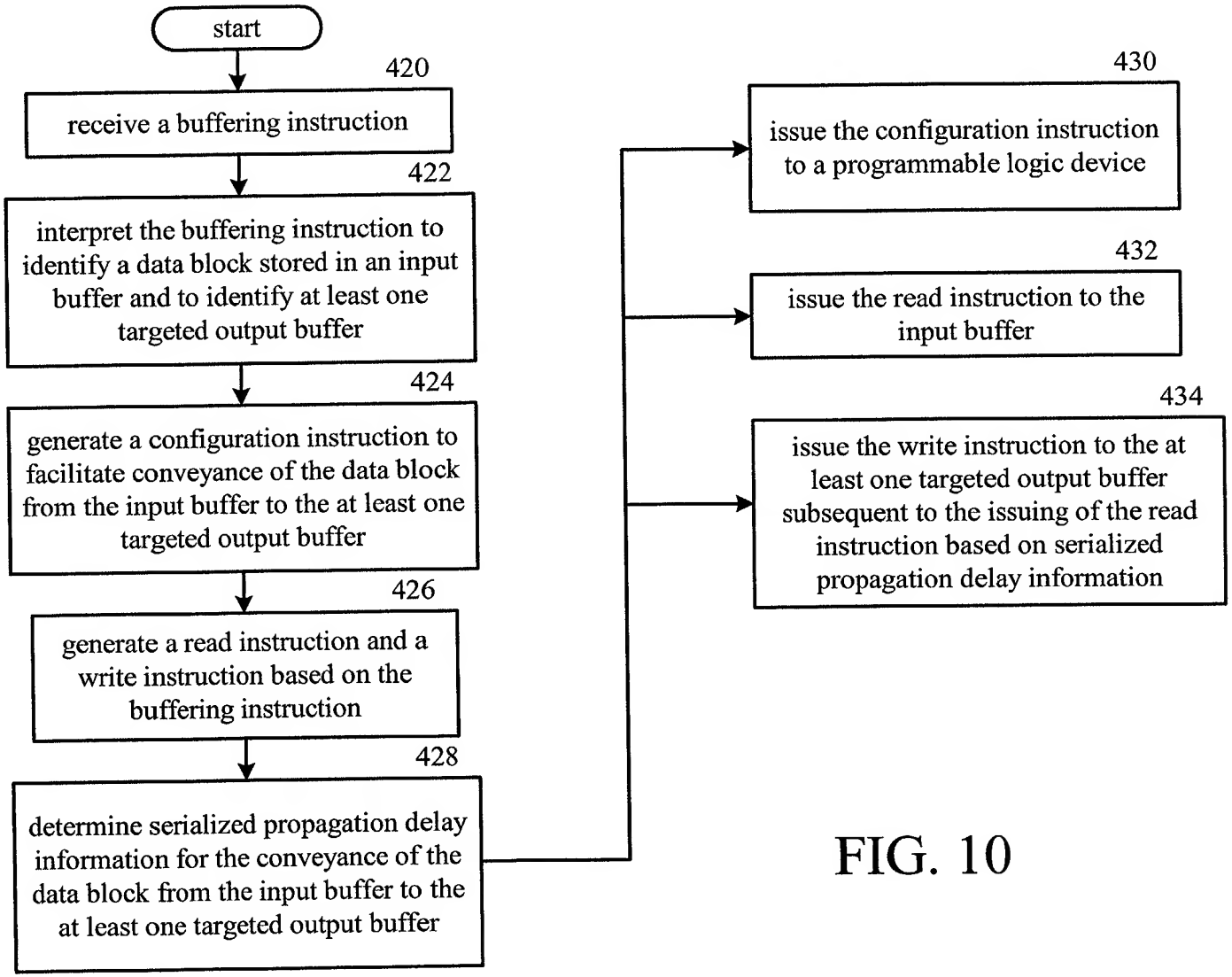
start
420
receive a buffering instruction
422
interpret the buffering instruction to identify a data block stored in an input buffer and to identify at least one targeted output buffer
424
generate a configuration instruction to facilitate conveyance of the data block from the input buffer to the at least one targeted output buffer
426
generate a read instruction and a write instruction based on the buffering instruction
428
determine serialized propagation delay information for the conveyance of the data block from the input buffer to the at least one targeted output buffer
430
issue the configuration instruction to a programmable logic device
432
issue the read instruction to the input buffer
434
issue the write instruction to the at least one targeted output buffer subsequent to the issuing of the read instruction based on serialized propagation delay information

FIG. 10

Photo: 10026001

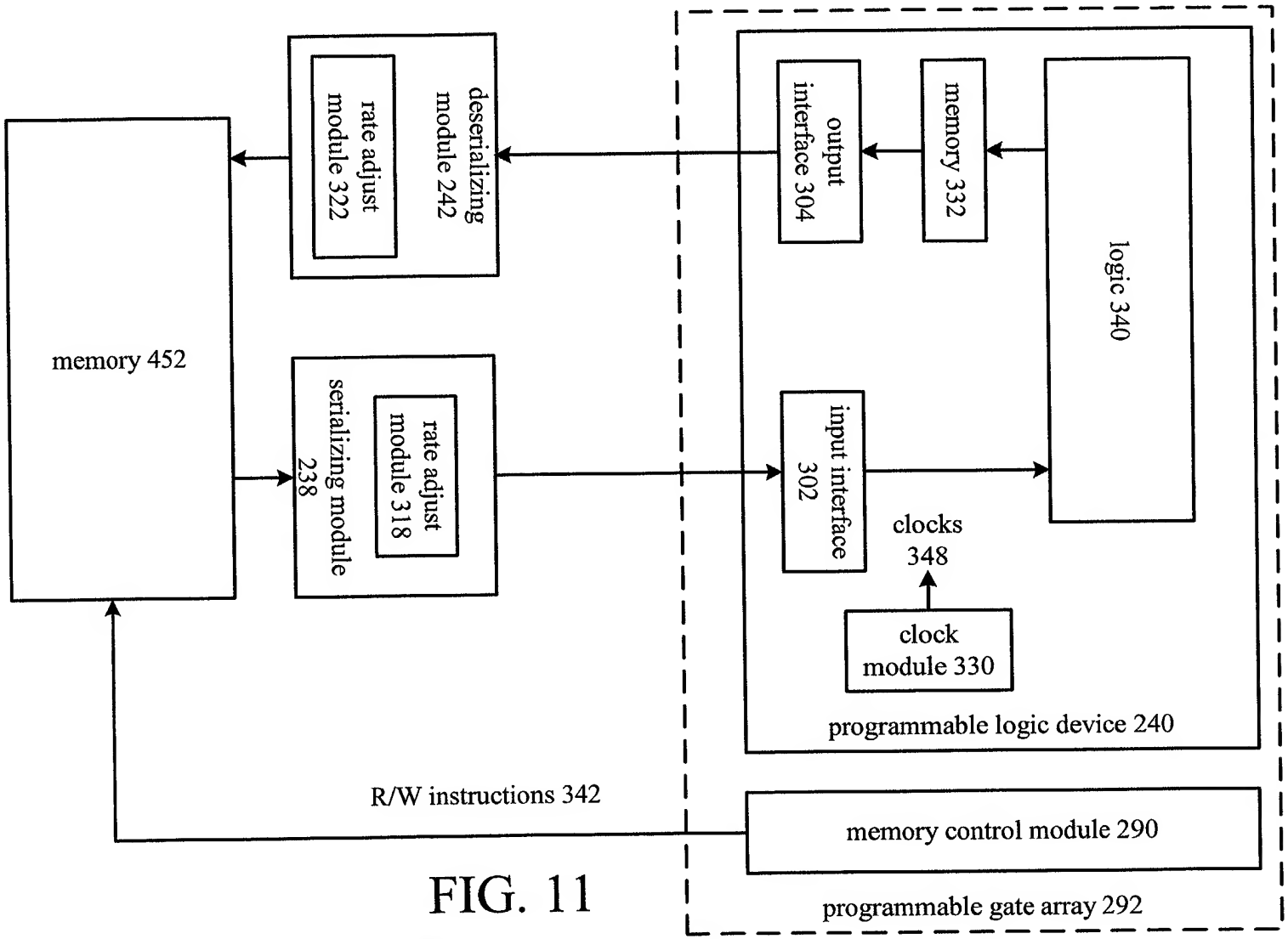

FIG. 11

buffer system 450